REMARKS

Claims 1-68 were pending. Claims 1-10, 30-42, and 65-68 have been cancelled. Claims 69-93 have been added. Claims 11, 12, 17-19, 24, 25, 27, 29, 43, 53, 54, 56, 57, and 61-64 have been amended to clarify the nature of the invention. Support for these amendments may be found in the Specification in at least paragraphs [0034], [0039], [0049], and [0069]. Accordingly, claims 11-29, 43-64, and 69-93 remain pending subsequent entry of the present amendment.

Claims 30-42 and 61-68 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Claims 30-42 and 65-68 have been cancelled. Applicant respectfully requests removal of the remainder of these rejections in view of the present amendments to claims 61-64.

Claims 1-41, 43-48, and 50-68 are rejected under 35 U.S.C. §102(b) as being anticipated by Carpenter (U.S. patent No. 6,067,611, hereinafter "Carpenter"). Applicant respectfully traverses these rejections and requests reconsideration in view of the following remarks.

In the present Office Action, it is suggested that Carpenter discloses all of the features of claim 11. However, Applicant disagrees. By way of preface, Applicant notes the nature of the presently claimed invention is quite distinct from that disclosed by Carpenter. For example, the snoop as recited in the claims is different from that disclosed by Carpenter. In Carpenter, a node controller within a node simply snoops transactions on a local interconnect 16 and/or an interconnect 22. In contrast, the recited snoop comprises the global arbiter querying a plurality of agents to determine whether that have data associated with a request received by the global arbiter. The global arbiter may then receive a number of associated responses to the query from a plurality of agents. In particular, as highlighted above in claim 11, the global arbiter is configured to execute a snoop corresponding to each request, wherein each snoop comprises determining whether one or more of the plurality of microprocessors has data associated with a corresponding

request. In addition to the differing natures of the recited snoop and the snoop disclosed by Carpenter, the recited global arbiter and disclosed central arbiter 27 of Carpenter perform completely different functions. Carpenter merely discloses a central arbiter for granting bus access. In contrast, the recited global arbiter receives one or more requests for a memory transaction, assigns a global order to the requests, and determines whether one or more of the microprocessors has associated data. The central arbiter of Carpenter performs none of these functions.

Turning now to the rejections, it is stated (pages 5-6):

> "Carpenter discloses a microprocessor based system comprising: a first microprocessor having a cache for caching data from a memory [Figure 1, #10a], said first microprocessor having a bus interface that implements a plurality of bus phases for a memory transaction [Column 3, Lines 38-48 & Column 4, Lines 1-12]; a second microprocessor having a cache for caching data from said memory, said second microprocessor having a bus interface that implements a plurality of bus phases for a memory transaction [Figure 1, #10b]; a memory controller, coupled to said memory [Figure 1, #20 & # 24], and a global arbiter, coupled to said bus interface of said first microprocessor , to said bus interface of said second microprocessor, and to said memory controller [Figure 2A, #27], said global arbiter for receiving requests for memory transactions from said first and second microprocessors [Figure 2A, #12a-#12d], and for globally ordering said requests during request phases of said plurality of bus phases, and for initiating snoop phases to said bus interfaces to insure coherency [Column 2, Lines 40-60, Column 5, Lines 6-51], said snoop phases conforming to the globally ordering [Column 6, Lines 16-27]; wherein said snoop phases are latency independent with respect to said request phases [Column 2, Lines 17-28]."

However, Applicant submits that claim 11, as amended, recites features neither taught nor suggested by Carpenter. Amended claim 11 recites:

> "A microprocessor based system comprising:
>
> a memory controller coupled to a memory and to a plurality of microprocessors, each microprocessor having a bus interface that implements a plurality of bus phases for a memory transaction; and
>
> a global arbiter, coupled to each bus interface and to said

memory controller, wherein said **global arbiter is configured to:**
receive one or more requests for a memory transaction;
assign a global order to each of the one or more requests;
execute according to the global order, a snoop corresponding to each request, wherein each snoop comprises determining whether one or more of the plurality of microprocessors has data associated with a corresponding request; and
respond to each request according to the global order."

As discussed above, the global arbiter is configured to execute a snoop corresponding to each request, wherein each snoop comprises determining whether one or more of the plurality of microprocessors has data associated with a corresponding request. Carpenter merely discloses a central arbiter for granting bus access. More particularly, Carpenter discloses:

"Referring now to FIG. 2A, a preferred embodiment of node interconnect 22 within NUMA computer system 8 is illustrated from the perspective of one of processing nodes 10. As shown, the illustrated embodiment of node interconnect 22 includes separate (i.e., non-multiplexed) address and data portions, which are decoupled to permit split transactions. The address portion of node interconnect 22 is implemented as a shared address bus 26, access to which is controlled by central arbiter 27. A node controller 20 requests access to shared address bus 26 by asserting its respective address bus request (ABR) signal 25 and is informed of a grant of access by central arbiter 27 through the assertion of its respective address bus grant (ABG) signal 29. Each node controller 20 coupled to node interconnect 22 also snoops all communication transactions on shared address bus 26 to support memory coherency, as discussed further below." (Carpenter col. 5, lines 6-24).

Further, as may be seen from the above, Carpenter discloses that each node controller snoops all communication transactions on shared address bus 26 to support memory coherency. Therefore, Carpenter discloses a snoop technique that is completely different from the snoop of claim 11. Not only is the nature of the recited snoop different

from that disclosed by Carpenter, but also the central arbiter of Carpenter does not perform the functions of the recited global arbiter. Accordingly, Applicant finds no teaching or suggestion in Carpenter of "a global arbiter, . . . configured to: receive one or more requests for a memory transaction; assign a global order to each of the one or more requests; execute according to the global order, a snoop corresponding to each request, wherein each snoop comprises determining whether one or more of the plurality of microprocessors has data associated with a corresponding request . . .," as is recited in claim 11.

For at least the above reasons, Applicant submits claim 11 is patentably distinct from Carpenter. As independent claims 43, 53, 61, and 72 include features similar to that of claim 11, claims 43, 53, 61, and 72 are patentably distinguished as well. Likewise, as each of dependent claims 12-29, 44-52, 54-60, 62-64, 69-71, and 73-93 includes the features of the independent claims upon which it depends, each of the dependent claims is believed patentable for at least the above reasons as well.

In addition to the above, Applicant submits that the dependent claims recite features neither taught nor suggested by the cited art. For example, claim 17 recites "[t]he microprocessor based system as recited in claim 11 wherein said determining comprises communicating a query corresponding to a request to each of the plurality of microprocessors." Since the global arbiter performs "said determining", it is readily apparent that the global arbiter also communicates a query corresponding to each request to each of the plurality of microprocessors. These features are not found anywhere in Carpenter. Accordingly, claim 17 is believed patentably distinct from the cited art for at least these additional reasons. As claims 56, 61, 70, and 74 include features similar to that of claim 17, claims 56, 61, 70, and 74 are patentably distinguished as well.

In addition, claim 25 recites " The microprocessor based system as recited in claim 11 wherein said determining comprises: communicating a query corresponding to a given request to each of the plurality of microprocessors; and waiting

until a response to the query corresponding to the given request is received from each of the plurality of microprocessors before responding to the given request." These features are also not found anywhere in Carpenter. Accordingly, claim 25 is believed patentably distinct from the cited art for at least these additional reasons. As claims 57, 63, 71, and 75 include features similar to that of claim 25, claims 57, 63, 71, and 75 are patentably distinguished as well.

Also, claims 42 and 49 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Carpenter in view of Mowery et al. (U.S. Patent No. 6,898,766). In view of the above remarks, Applicant submits that further traversal of these rejections is unnecessary at this time.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

Respectfully submitted,

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